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(FILE 'HOME' ENTERED AT 14:29:18 ON 21 FEB 2002)

FILE 'EUROPATFULL, PCTFULL, USPATFULL, USPAT2' ENTERED AT 14:29:27 ON 21 FEB 2002

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L1        44887 S (SEPARAT? OR FIELD OR LOCOS)(3W)(OXIDE# OR INSULAT?)
L2      1468812 S HEAT? OR ANNEAL?
L3      1163238 S INERT OR NITROGEN OR N2 OR N(3W)2 OR HYDROGEN OR H2 OR
H(3W)2
L4      1229896 S L3 OR ARGON OR AR
L5         3618 S L1(P)L2(P)L4
                SET HIGH OFF
L6       409458 S STRESS##
                SET HIGH ON
L7          939 S L5 AND L6
                SET HIGH OFF
L8        10256 S LOCOS OR LOCAL?(4W)(OXIDI? OR OXIDAT?)
                SET HIGH ON
L9          188 S L7 AND L8
L10         266 S L1(30A)L2(30A)L4
L11          68 S L10 AND L8
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=> d 16 18 24 25 27 29 30 31 39 47 49 64 bib ab

L11 ANSWER 16 OF 68 USPATFULL

AN 2001:134057 USPATFULL

TI METHOD FOR FORMING AN ISOLATION REGION IN A SEMICONDUCTOR DEVICE AND RESULTING STRUCTURE USING A TWO STEP OXIDATION PROCESS

IN JANG, SE AUG, ICHON-SHI, Korea, Republic of
KIM, YOUNG BOG, ICHON-SHI, Korea, Republic of
YEO, IN SEOK, ICHON-SHI, Korea, Republic of
KIM, JONG CHOUL, ICHON-SHI, Korea, Republic of

PI US 2001014506 A1 20010816

AI US 1998-62291 A1 19980417 (9)

Date no good

PRAI KR 1997-22708 19970602

DT Utility

FS APPLICATION

LREP ROBERT C COLWELL, TOWNSEND TOWNSEND & CREW, TWO EMBARCADERO CENTER, EIGHTH FLOOR, SAN FRANCISCO, CA, 941113834

CLMN Number of Claims: 19

ECL Exemplary Claim: 1

DRWN 15 Drawing Page(s)

LN.CNT 675

CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AB A method for forming an element isolation film of a semiconductor device and the semiconductor device. A pad insulator is constructed on a semiconductor substrate. An over-etching process is performed to recess the semiconductor substrate to a predetermined depth while giving a pad insulator pattern. After an insulator spacer is formed at the side wall of the pad insulator pattern, the exposed region of the semiconductor substrate is thermally oxidized to grow an oxide which is, then, removed to form a recess. An element isolation film is formed in the recess by break-through field oxidation and high temperature field oxidation. The element isolation film thus obtained can prevent the field oxide "ungrowth" phenomenon and at the same time mitigate the field oxide

thinning effect as well as improve the properties of the gate oxide.

L11 ANSWER 18 OF 68 USPATFULL
AN 2001:47911 USPATFULL
TI Locos processes
IN Kwok, Siang Ping, Dallas, TX, United States
PA Micron Technology, Inc., Boise, ID, United States (U.S. corporation)
PI US 6211037 B1 20010403
AI US 1999-387661 19990830 (9)
DT Utility
FS Granted
EXNAM Primary Examiner: Nelms, David; Assistant Examiner: Nhu, David
LREP Wells, St. John, Roberts, Gregory & Matkin, P.S.
CLMN Number of Claims: 21
ECL Exemplary Claim: 1
DRWN 8 Drawing Figure(s); 4 Drawing Page(s)
LN.CNT 306
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB The invention includes a method of reducing stress during formation of field oxide by LOCOS. Field oxide is formed by oxidizing a silicon substrate, and fluorine is incorporated into the field oxide during the oxidizing. After the fluorine is incorporated into the field oxide, the field oxide is annealed at a temperature of at least about 1000.degree. C.

L11 ANSWER 24 OF 68 USPATFULL
AN 2000:4724 USPATFULL
TI Method for forming field oxide film of semiconductor device
IN Jang, Se Aug, Ichon, Korea, Republic of
Cho, Byung Jin, Ichon, Korea, Republic of
Kim, Jong Choul, Ichon, Korea, Republic of
PA Hyundai Electronics Industries Co., Ltd., Kyoungki-do, Korea, Republic of (non-U.S. corporation)
PI US 6013561 20000111
AI US 1997-961132 19971030 (8)
PRAI KR 1996-68904 19961220
DT Utility
FS Granted
EXNAM Primary Examiner: Dang, Trung
LREP Thelen Reid & Priest, LLP
CLMN Number of Claims: 15
ECL Exemplary Claim: 9
DRWN 10 Drawing Figure(s); 7 Drawing Page(s)
LN.CNT 417
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB A method for forming a field oxide film of a highly integrated semiconductor device, in which an annealing step is carried out during a field oxide film formation step for growing the field oxide film adapted to isolate elements of the semiconductor device. By the annealing step, it is possible to prevent a stress concentration phenomenon from occurring in a semiconductor substrate on which the field oxide film is formed, thereby reducing or eliminating a field oxide thinning phenomenon.

L11 ANSWER 25 OF 68 USPATFULL
AN 2000:4720 USPATFULL
TI Advanced CMOS isolation utilizing enhanced oxidation by light ion implantation
IN Wu, Zhiqiang Jeff, Meridian, ID, United States
Li, Li, Meridian, ID, United States
PA Micron Technology, Inc., Boise, ID, United States (U.S. corporation)
PI US 6013557 20000111
AI US 1998-136240 19980819 (9)
RLI Continuation of Ser. No. US 1996-691571, filed on 2(Aug)(1996), now

patented, Pat. No. US 5863826
DT Utility
FS Granted
EXNAM Primary Examiner: Fourson, George
LREP Knobbe, Martens, Olson & Bear, LLP
CLMN Number of Claims: 34
ECL Exemplary Claim: 1,9
DRWN 16 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 579
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB A method for forming field isolation regions in multilayer semiconductor devices comprises the steps of masking active regions of the substrate, forming porous silicon in the exposed field isolation regions, removing the mask and oxidizing the substrate. A light ion impurity implant is used to create pores in the substrate. Substrate oxidation proceeds by rapid thermal annealing because the increased surface area of the pores and the high reactivity of unsaturated bonds on these surfaces provides for enhanced oxidation.

L11 ANSWER 27 OF 68 USPATFULL
AN 1999:159896 USPATFULL
TI Modified recessed locos isolation process for deep sub-micron device processes
IN Bergemont, Albert, Palo Alto, CA, United States
Owens, Alexander H., Los Gatos, CA, United States
PA National Semiconductor Corporation, Santa Clara, CA, United States (U.S. corporation)
PI US 5998280 19991207
AI US 1998-45226 19980320 (9)
DT Utility
FS Granted
EXNAM Primary Examiner: Dang, Trung
LREP Skjerven, Morrill, MacPherson Franklin and Friel, Halbert, Michael J.
CLMN Number of Claims: 16
ECL Exemplary Claim: 1
DRWN 8 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 338
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB A trench is etched in a silicon substrate covered with an oxide/nitride stack and a field oxide layer is then grown through oxidation of the silicon in the substrate such that the trench is partly filled. There is reduced oxide encroachment into the active areas under the nitride layer because of the partial field oxide growth. Double oxide layers are deposited over the surface of the field oxide layer and the oxide/nitride stack such that the oxide layers fill the remainder of the trench and produce a nearly planar topology. The double oxide layers are then etched back to the nitride layer through chemical mechanical polishing, leaving the field isolation region. After stripping the oxide/nitride stack, a gate oxide layer is grown. A minimal amount of oxide is required to fill the trench because the trench is already almost filled with the field oxide layer and because of the shallow depth of the trench. Consequently, the etch back step causes minimal dishing. Further, the field oxide layer rounds the corner between the trench and the active area, obviating the need for a thin oxide liner in the trench.

L11 ANSWER 29 OF 68 USPATFULL
AN 1999:132666 USPATFULL
TI Method for forming field oxide film of semiconductor device with silicon

and nitrogen containing etching residue
IN Jang, Se Aug, Kyoungki-do, Korea, Republic of
PA Hyundai Electronics Industries, Kyoungki-do, Korea, Republic of (non-U.S. corporation)
PI US 5972779 19991026
AI US 1997-965893 19971107 (8)
PRAI KR 1996-80220 19961231
DT Utility
FS Granted
EXNAM Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Mao, Daniel H.
LREP Thelen Reid & Priest, L.L.P.
CLMN Number of Claims: 11
ECL Exemplary Claim: 1
DRWN 23 Drawing Figure(s); 11 Drawing Page(s)
LN.CNT 414
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB A field oxide formation method involving a primary field oxidation, which is carried out at a predetermined low temperature to form a field oxide film having a thickness smaller than a target thickness, and a secondary field oxidation, which is carried out at a higher temperature capable of relatively reducing the occurrence of a field thinning phenomenon, to form the remaining thickness portion of the target field oxide film. The field thinning phenomenon involved in a field oxidation is reduced. The characteristics of a finally produced gate oxide film is also improved. Consequently, the throughput and reliability of semiconductor devices having gate oxide films are improved.

L11 ANSWER 30 OF 68 USPATFULL
AN 1999:47700 USPATFULL
TI Field oxidation by implanted oxygen (FIMOX)
IN Lur, Water, Taipei, Taiwan, Province of China
Huang, Cheng Han, Hsin-chu, Taiwan, Province of China
PA United Microelectronics Corporation, Taiwan, Taiwan, Province of China (non-U.S. corporation)
PI US 5895252 19990420
AI US 1995-552209 19951102 (8)
RLI Continuation of Ser. No. US 1994-239425, filed on 6 May 1994, now abandoned
DT Utility
FS Granted
EXNAM Primary Examiner: Fourson, George
LREP Rabin & Champagne, P.C.
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 7 Drawing Figure(s); 3 Drawing Page(s)
LN.CNT 382
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB A method of forming a field oxide isolation region is described, in which a masking layer is formed over a silicon substrate. The masking layer is patterned to form an opening for the field oxide isolation region, whereby the remainder of the masking layer forms an implant mask. A conductivity-imparting dopant is implanted through the opening into the silicon substrate. Oxygen is implanted through the opening into the silicon substrate in multiple implantation steps. The implant mask is removed. The field oxide isolation region is formed in and on the silicon substrate, by annealing in a non-oxygen ambient. Alternately, the field oxide isolation region is formed by annealing in oxygen, simultaneously forming a gate oxide in the region between the field oxide isolation regions.

L11 ANSWER 31 OF 68 USPATFULL
AN 1999:12836 USPATFULL
TI CMOS isolation utilizing enhanced oxidation of recessed porous silicon formed by light ion implantation

IN Wu, Zhiqiang Jeff, Meridian, ID, United States
Li, Li, Meridian, ID, United States
PA Micron Technology, Inc., Boise, ID, United States (U.S. corporation)
PI US 5863826 19990126
AI US 1996-691571 19960802 (8)
DT Utility
FS Granted
EXNAM Primary Examiner: Fourson, George R.
LREP Knobbe, Martens, Olson & Bear, LLP
CLMN Number of Claims: 32
ECL Exemplary Claim: 31
DRWN 16 Drawing Figure(s); 8 Drawing Page(s)
LN.CNT 596
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB A method for forming field isolation regions in multilayer semiconductor devices comprises the steps of masking active regions of the substrate, forming porous silicon in the exposed field isolation regions, removing the mask and oxidizing the substrate. A light ion impurity implant is used to create pores in the substrate. Substrate oxidation proceeds by rapid thermal annealing because the increased surface area of the pores and the high reactivity of unsaturated bonds on these surfaces provides for enhanced oxidation.

L11 ANSWER 39 OF 68 USPATFULL
AN 97:84225 USPATFULL
TI Semiconductor device with reduced leakage current
IN Kunikiyo, Tatsuya, Hyogo, Japan
PA Mitsubishi Denki Kabushiki Kaisha, Tokyo, Japan (non-U.S. corporation)
PI US 5668403 19970916
AI US 1996-706966 19960903 (8)
RLI Continuation of Ser. No. US 1995-397342, filed on 2 Mar 1995, now abandoned
PRAI JP 1994-178408 19940729
DT Utility
FS Granted
EXNAM Primary Examiner: Ngo , Ngan V.
LREP Lowe, Price, LeBlanc & Becker
CLMN Number of Claims: 7
ECL Exemplary Claim: 1
DRWN 43 Drawing Figure(s); 21 Drawing Page(s)
LN.CNT 785
AB The present invention provides a method of manufacturing a semiconductor device improved so that stress at a boundary between a semiconductor substrate and an element isolation oxide film can be relaxed. In the method, the surface of a semiconductor substrate is oxidized with a nitride film used as a mask to form an element isolation oxide film in the surface of semiconductor substrate. After removing an underlay oxide film and nitride film, semiconductor substrate is heat-treated at a temperature of 950.degree. C. or more. An element is formed in an element region.

L11 ANSWER 47 OF 68 USPATFULL
AN 95:18363 USPATFULL
TI "Bird-beak-less" field isolation method
IN Ko, Joe, Hsinchu, Taiwan, Province of China
Lin, Chih-Hung, I-Lai, Taiwan, Province of China
PA United MicroElectronics Corporation, Hsinchu, Taiwan, Province of China (non-U.S. corporation)
PI US 5393693 19950228
AI US 1994-254533 19940606 (8)
DT Utility
FS Granted
EXNAM Primary Examiner: Fourson, George

LREP Saile, George O.; Ackerman, Stephen B.
CLMN Number of Claims: 19
ECL Exemplary Claim: 1,9
DRWN 14 Drawing Figure(s); 5 Drawing Page(s)
LN.CNT 400
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB A method of forming field oxide isolation regions for submicron technology using oxygen implantation is described. A first insulating layer is formed over a silicon substrate. A second insulating layer is formed over the first insulating layer. A first opening is formed in the first and second insulating layers. Sidewall spacers are formed on the vertical surfaces of the first and second insulating layers, within the first opening, to define a second, smaller opening. A portion of the silicon substrate is removed in the region defined by the second, smaller opening, to form an etched region of the silicon substrate. The sidewall spacers are removed. Oxygen is implanted into the etched region of the silicon substrate and into the region of the silicon substrate under the former location of the sidewall spacers. A portion of the polycrystalline silicon in and above the etched region of the silicon substrate. The field oxide isolation region is formed by heating. The remainder of the first and second insulating layers are removed.

L11 ANSWER 49 OF 68 USPATFULL
AN 94:46922 USPATFULL
TI Method of decreasing the field oxide etch rate in isolation technology
IN Philipossian, Ara, Redwood Shores, CA, United States
Soleimani, Hamid R., Westborough, MA, United States
Doyle, Brian S., Framington, MA, United States
PA Digital Equipment Corporation, Maynard, MA, United States (U.S. corporation)
PI US 5316965 19940531
AI US 1993-99136 19930729 (8)
DT Utility
FS Granted
EXNAM Primary Examiner: Hearn, Brian E.; Assistant Examiner: Dang, Trung
LREP Feltovic, Robert J., Maloney, Denis G., Cefalo, Albert P.
CLMN Number of Claims: 23
ECL Exemplary Claim: 1
DRWN 8 Drawing Figure(s); 2 Drawing Page(s)
LN.CNT 330
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB An improved process for planarizing an isolation barrier in the fabrication of a semiconductor chip involves reducing the etch rate of the **field oxide** independently of the sacrificial oxide layer. The **field oxide** layer is implanted with **nitrogen** ions and then thermally **annealed** resulting in a hardened and densified **field oxide**. In subsequent operations, a sacrificial oxide layer is formed on the semiconductor top surface by thermal oxidation. Upon etching with HF, the etch rate of the hardened field oxide is significantly reduced relative to untreated field oxide. Thus, the exposed hardened field oxide is etched at about the same rate as the sacrificial oxide layer. In the example given, the etch rate of untreated densified TEOS field oxide in 10:1 HF is 6.90 .ANG./sec, while the etch rate of TEOS field oxide hardened according to the processes of this invention is 5.90 .ANG./sec. After planarization using the hardened field oxide, depressions in the isolation barrier are eliminated.

L11 ANSWER 64 OF 68 USPATFULL
AN 88:13193 USPATFULL

TI Field implant process for CMOS using germanium
IN Pfiester, James [redacted], Austin, TX, United States
Alvis, John R., Austin, TX, United States
Holland, Orin W., Oak Ridge, TN, United States
PA Motorola, Inc., Schaumburg, IL, United States (U.S. corporation)
PI US-4728619 19880301
AI US 1987-63934 19870619 (7)
DT Utility
FS Granted
EXNAM Primary Examiner: Roy, Upendra
LREP Fisher, John A., Van Myers, Jeffrey, Mossman, David L.
CLMN Number of Claims: 22
ECL Exemplary Claim: 1
DRWN 20 Drawing Figure(s); 14 Drawing Page(s)
LN.CNT 834
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

AB A complementary metal-oxide-semiconductor (CMOS) isolation structure where the field isolation structure between the adjacent areas of different conductivity types has a channel stop doped with boron or phosphorus affected by germanium. The dual use of germanium and a second dopant selected from the group of phosphorus and boron provides a more precisely placed channel stop, since the germanium retards the diffusion of the boron and phosphorus and surprisingly provides improved width effect for the devices in the well where the channel stop is employed. Alternatively, the germanium may be placed in such a manner as to avoid retarding absorption of boron or phosphorus into the field oxide and retard its diffusion over the well of a different conductivity type where it is not desired.

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FILE 'EUROPATFULL, PCTFULL, USPATFULL, USPAT2' ENTERED AT 14:29:27 ON 21 FEB 2002

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L1         44887 S (SEPARAT? OR FIELD OR LOCOS)(3W)(OXIDE# OR INSULAT?)
L2       1468812 S HEAT? OR ANNEAL?
L3       1163238 S INERT OR NITROGEN OR N2 OR N(3W)2 OR HYDROGEN OR H2 OR
H(3W)2
L4       1229896 S L3 OR ARGON OR AR
L5          3618 S L1(P)L2(P)L4
                 SET HIGH OFF
L6        409458 S STRESS##
                 SET HIGH ON
L7           939 S L5 AND L6
                 SET HIGH OFF
L8         10256 S LOCOS OR LOCAL?(4W)(OXIDI? OR OXIDAT?)
                 SET HIGH ON
L9           188 S L7 AND L8
L10          266 S L1(30A)L2(30A)L4
L11           68 S L10 AND L8
                 SET HIGH OFF
L12         3641 S PAD(3W)OXIDE#
                 SET HIGH ON
L13           39 S L10 AND L12
L14            8 S L13 NOT L11
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=> d 2 4 bib ab

L14 ANSWER 2 OF 8 USPATFULL
AN 2001:220963 USPATFULL
TI Semiconductor device and production thereof
IN Miura, Hideo, Koshigaya, Japan
Ikeda, Shuji, Koganei, Japan
Suzuki, Norio, Higashimurayama, Japan
Hagiwara, Yasuhide, Fuchu, Japan
Ohta, Hiroyuki, Tsuchiura, Japan
Nishimura, Asao, Kokubunji, Japan
PA Hitachi, Ltd., Tokyo, Japan (non-U.S. corporation)
PI US 6326284 B1 20011204
AI US 1996-610488 19960304 (8)
PRAI JP 1995-48106 19950308
DT Utility
FS GRANTED
EXNAM Primary Examiner: Dang, Trung
LREP Antonelli, Terry, Stout & Kraus, LLP
CLMN Number of Claims: 7
ECL Exemplary Claim: 1
DRWN 26 Drawing Figure(s); 10 Drawing Page(s)
LN.CNT 720
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

parent case

AB A semiconductor device produced by forming an oxide film on a substrate, heat treating the oxide film at a temperature of 800.degree. C. or higher in an inert atmosphere, followed by conventional steps for formation of a transistor, is improved in electrical reliability due to relaxation of stress generated in the oxide film or in the surface of

substrate.

L14 ANSWER 4 OF 8 USPATFULL
AN 1999:146437 USPATFULL
TI Method for forming field oxide of semiconductor device using wet and dry
oxidation
IN Jang, Se Aug, Ichon, Korea, Republic of
Kim, Young Bog, Ichon, Korea, Republic of
Joo, Moon Sig, Ichon, Korea, Republic of
Cho, Byung Jin, Ichon, Korea, Republic of
Kim, Jong Choul, Ichon, Korea, Republic of
PA Hyundai Electronics Industries Co., Ltd., United States (U.S. corporation)
PI US 5985738 19991116
AI US 1997-959205 19971028 (8)
PRAI KR 1996-49395 19961029
DT Utility
FS Granted
EXNAM Primary Examiner: Chaudhuri, Olik; Assistant Examiner: Mao, Daniel
LREP Thelen Reid & Priest, L.L.P.
CLMN Number of Claims: 10
ECL Exemplary Claim: 1
DRWN 23 Drawing Figure(s); 10 Drawing Page(s)
LN.CNT 325
CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AB A method for forming a field oxide of a semiconductor device is disclosed, which takes advantage of wet oxidation at an early stage of field oxidation to prevent the ungrowth of field oxide and dry oxidation at a later stage of field oxidation to make the slope of field oxide positive, thereby improving the production yield and the reliability of semiconductor device.